REMARKS

Claims 1–7 and 27–39 are pending in the present application.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, First Paragraph (Written Description)

Claim 27 was rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification in such a way to to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. This rejection is respectfully traversed.

The Office Action asserts that first and second sidewall spacers (formed on the same side of the gate electrode) is not described. However, as depicted in Figures 8–11 and described in the specification, first and second conformal, undoped oxide insulating layers 29 and 48 are patterned to form first and second sidewall spacers 38 and 50, or at least "inner" and "outer" portions of an overall sidewall spacer structure. The specification thus contains ample written support for the limitation at issue.

Therefore, the rejection of claim 27 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 112, Second Paragraph (Definiteness)

Claims 1–7 and 28–39 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. This rejection is respectfully traversed.

The standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope. MPEP § 2173.02; *In re Warmerdam*, 33 F.3d 1354, 1361, 31 U.S.P.Q.2d 1754, 1759 (Fed. Cir. 1994). Determining whether a claim is indefinite requires an analysis of whether one skilled in the art would understand the bounds of the claim when read in light of the specification. *Credle v. Bond*, 25 F.3d 1566, 1576, 30 U.S.P.Q.2d 1911, 1919 (Fed. Cir. 1994). The claim is not indefinite if one skilled in the art would have no particular difficulty in determining whether the claimed features have been implemented. *In re Warmerdam*, 33 F.3d 1354, 1361, 31 U.S.P.Q.2d 1754, 1759 (Fed. Cir. 1994). The claim limitation is sufficient if it enables those skilled in the art to draw a line between embodiments falling within the scope of the claim and those which do not. *In re Marosi*, 710 F.2d 799, 802-03, 218 U.S.P.Q. 289, 292 (Fed. Cir. 1983).

The Office Action objects to the claim limitation of "a minimum channel length required for the p-channel transistors" or "a distance below which the transistor will not operate reliably due to short channel effects." As noted in the specification:

> [A] MOS device, manufactured using CMOS technology, is reliable when the distance 70 between its source and drain 44', i.e. its channel length, is between a minimum length and a maximum length. The minimum length is a distance between the source and drain of the transistor below which the transistor will not

> operate reliably due to short channel effects when a conventional voltage is applied to the gate electrode.

Specification, page 10, lines 8–13. The specification also notes the variable gate voltages (5, 3.3 and 2.7) commonly employed, and that minimum channel length typically depends primarily on doping concentration in the LDD regions. For these reasons, semiconductor design rules specify minimum channel lengths for particular fabrication processes and device structures (particularly doping profiles). However, those skilled in the art would have no difficultly ascertaining the minimum required channel length from the enterprise design rules for a particular process.

Similarly, the Office Action objects to recitation in the claims of "a distance above which the transistor will not turn on efficiently." The specification teaches that a transistor will not turn on efficiently when current does not flow between the source and drain of the transistor when a conventional voltage (5, 3.3 or 2.7) is applied to the gate electrode of the transistor. Specification, page 10, lines 15–17. Those skilled in the art would have no particular difficulty determining whether such a limitation is satisfied in the claims.

The Office Action also objects to "a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor." Dopant diffusion is well understood by those skilled in the relevant art, and must of necessity be calculated in designing a fabrication process.

Therefore, the rejection of claims 1–7 and 28–39 under 35 U.S.C. § 112, second paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 33–34 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,273,914 to *Miyajima et al.* Claim 27–30 and 32 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,766,991 to *Chen*. These rejections are respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

As previously noted, independent claim 27 recites that first and second sidewalls overlie a portion of the channel and portions of the source and drain regions of the p-channel transistor, in combination with an n-channel transistor having lightly doped source/drain regions. Such a feature is not depicted or described by the cited references. *Miyajima et al* does not describe such a feature, while *Chen* teaches removing the (second) silicon nitride sidewalls 76 through

79 prior to implanting lightly doped regions for the n-channel transistor. *Chen*, column 6, lines 64–65.

As previously noted, claim 28 recites that the p-channel gate electrode is smaller than a minimum channel length required for the p-channel transistor. The present invention uses multiple insulating layers to mask implantation of LDD regions in order to form a structure having a gate electrode shorter than the minimum channel length required. Such a feature is not depicted or described by the cited references. Both references depict structures in which the gate electrode is shorter than the channel length, but neither reference teaches that the gate electrode is shorter than the minimum viable channel length for the fabrication process utilized.

Similarly, independent claim 33 recites a gate electrode for the p-channel transistor having a width smaller than the minimum channel length for the p-channel transistor and covered by at least one conformal insulating layer with a thickness that, taken twice (once on each side of the gate electrode) and added to the width of the gate electrode, exceeds the minimum channel length. In the present invention, implantation of the source/drain regions for the p-channel transistor are masked by the gate electrode and an overlying (first) conformal insulating layer. A subsequent diffusion drives the impurities under sidewall spacers formed from the first insulating layer Such a feature is not depicted or described by either reference.

Therefore, the rejections of claims 27–30 and 32–34 under 35 U.S.C. § 102 have been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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